second drain of which is connected to the self-biased transistor for receiving a reference signal, wherein a first source of the first transistor and a second source of the second transistor are connected in common, and the differential circuit generates an internal signal at the first drain in accordance with a current flowing through the first and second transistors;

a constant current source connected to the first source of the first transistor; and

a current regulating circuit connected to the second source of the second transistor and connected in parallel to the constant current source, wherein the current regulating circuit increases and decreases an amount of the current flowing through the differential circuit in response to the internal signal wherein the internal signal is directly provided to the current regulating circuit.

4. (Amended) The input circuit according to claim 1, wherein the constant current source is connected to a high potential power supply, and wherein the current regulating circuit includes a third transistor connected in parallel to the constant current source, the third transistor going ON and OFF in response to the internal signal.

5. (Amended) The input circuit according to claim 1, wherein the constant current source is connected to a low potential power supply, and wherein the current regulating circuit includes a third transistor connected in parallel to the constant current source, the third transistor going ON and OFF in response to the internal signal.

REMARKS

The Office Action dated December 4, 2001, has been received and carefully noted. The period for response having been extended from March 4, 2002, to April 4,